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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, LONG T	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 02/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/776,250	ANDO, KAZUMASA	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is responsive to the amendment filed on 11/30/05.

2. The objections to the drawings in the last office action have been overcome based on applicant's amendment to the drawings.

Claim Objections

3. Claims 19, 27 and 33-46 are objected to because of the following informalities:

Claim 19, lines 11, 27 and 32, "a first conductive" should be changed to --the first conductive-- (see line 8 of claim 19).

Claim 19, line 16, "the high" should be changed to --a high-- to avoid lacking antecedent basis.

Claim 19, line 20, "a second conductive" should be changed to --the second conductive-- (see line 14 of claim 19).

Claims 33, 35, 37 and 39-42 are objected to because they include the informalities of claim 19.

Also, in claim 35, lines 2 and 7, "a second conductive" should be changed to --the second conductive-- (see line 14 of claim 19).

Claim 27, lines 14, 29 and 34, "a first conductive" should be changed to --the first conductive-- (see line 11 of claim 27).

Claim 27, line 18, "the high" should be changed to --a high-- to avoid lacking antecedent basis.

Claim 27, line 23, "a second conductive" should be changed to --the second conductive-- (see line 17 of claim 27).

Claims 34, 36, 38 and 43-46 are objected to because they include the informalities of claim 27.

Also, in claim 36, lines 2 and 7, "a second conductive" should be changed to --the second conductive-- (see line 17 of claim 27).

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 22, 30, 41 and 45 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claims 22, 30, 41 and 45, the recitation "and/or" is indefinite because it is not clear if the recitation means for an "and" or for an "or". Clarification or appropriate correction is requested.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this

subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 18-34 and 39-46 are rejected under 35 U.S.C. 102(e) as being anticipated by Maejima et al. (USP 6,791,392).

With respect to claims 18 and 20-23, Figure 3 of the Maejima et al. reference discloses a voltage level shifter circuit, which includes: a level changer (IV1, IV2, DT, TP1, TP2, TN1, TN2, TN31, TN32) having a current block (transistors TN31 and TN32) having a first transistor (either transistor TN1 or TN2); an input signal (IN); a low power voltage supply (VDDL); a high power voltage supply (VDDH); a reference potential (ground); an output circuit (CMOS inverter IV3) for providing an output signal (OUT); a retaining circuit (CMOS inverter IV4, which is a feedback circuit from the output of the output circuit to the output of the level changer, and the connection of the output circuit IV3 and the feedback circuit IV4 forms an output retainer circuit). Note that the gate of the first transistor (TN31 or TN32) configured to be supplied with a first potential of the low voltage power supply (VDDL, by way of voltage divider TP3-R). Also note for claim 23, because the structure of the level shifter in Figure 3 of the Maejima reference is substantially similar as applicant's invention so the limitation regarding the timing operation in this claim is also met.

With respect to claim 19, 33 and 39-42, Figure 3 of the Maejima et al. reference discloses a voltage level shifter circuit, which includes: a level changer (IV1, IV2, DT, TP1, TP2, TN1, TN2, TN31, TN32) including an input signal (IN), a low voltage power supply (VDDL), a high voltage power supply (VDDH), a reference potential (ground), a first input circuit (IV1), a second input circuit (IV2), a first MOSFET (NMOS TN1), a second MOSFET (NMOS TN2), a third MOSFET (PMOS TP1), a fourth MOSFET (PMOS TP2), and a current block (TN31,

TN32) comprising a fifth MOSFET (NMOS TN31) and a sixth MOSFET (NMOS TN32), wherein the fifth and sixth MOSFETs (TN31, TN32) having their gates connected to the low voltage power supply (VDDL, by way of voltage divider TP3-R); an output circuit (CMOS inverter IV3) for providing an output signal (OUT); a retainer circuit (CMOS inverter IV4). Note that, for claim 42, because the structure of the level shifter in Figure 3 of the Maejima reference is substantially similar as applicant's invention so the limitation regarding the timing operation in this claim is also met.

With respect to claims 24-26 and 28-32, the Maejima et al. reference (Col. 1, lines 9-13) discloses a system, which includes: a low power voltage supply (VDDL); a high power voltage supply (VDDH); a reference potential (ground); a peripheral circuit (the one circuit system, see Col. 1, lines 9-13, which inherently is supplied with the first power supply VDDL), a voltage level shifter circuit (the level shift circuit which is shown in Figure 3), and an internal circuit (the another system, see Col. 1, lines 9-13, which inherently is supplied with the second power supply VDDH), wherein the voltage level shifter circuit comprises: a level changer (IV1, IV2, DT, TP1, TP2, TN1, TN2, TN31, TN32) having a current block (transistors TN31 and TN32) including a first transistor (either transistor TN1 or TN2); an input signal (IN); an output circuit (CMOS inverter IV3); a retaining circuit (CMOS inverter IV4, which is a feedback circuit from the output of the output circuit to the output of the level changer, and the connection of the output circuit IV3 and the feedback circuit IV4 forms an output retainer circuit). Note that the gate of the first transistor (TN31 or TN32) configured to be supplied with a first potential of the low voltage power supply (VDDL, by way of voltage divider TP3-R). Note that, for claim 26, it is clear from the operation of the circuitry Maejima et al. reference that when the there is no power

supply to the system (i.e., power supply is 0V) then the system is not operated, so the system is in standby period, and when there is power supply to the system then the system is in operation period; so the peripheral circuit (the one circuit system) is in standby when the there is no power to the low supply voltage (i.e., VDDL is 0V which is the reference potential). Also note that, for claim 31, because the structure of the level shifter in Figure 3 of the Maejima reference is substantially similar as applicant's invention so the limitation regarding the timing operation in this claim is also met. Also note that, for claim 32, for broadest reasonable interpretation, both the level shifter (Figure 3) and the another circuit system (Col. 1, lines 9-13) are reasonable to be considered to be a microcomputer (i.e., the microcomputer comprises the level shifter (Figure 3) and the another circuit system).

With respect to claims 27, 34 and 43-46, the Maejima et al. reference (Col. 1, lines 9-13) discloses a system, which includes: a low power voltage supply (VDDL); a high power voltage supply (VDDH); a reference potential (ground); a peripheral circuit (the one circuit system, see Col. 1, lines 9-13, which inherently is supplied with the first power supply VDDL), a voltage level shifter circuit (the level shift circuit which is shown in Figure 3), and an internal circuit (the another system, see Col. 1, lines 9-13, which inherently is supplied with the second power supply VDDH), wherein the voltage level shifter circuit comprises: a level changer (IV1, IV2, DT, TP1, TP2, TN1, TN2, TN31, TN32) including an input signal (IN), a first input circuit (IV1), a second input circuit (IV2), a first MOSFET (NMOS TN1), a second MOSFET (NMOS TN2), a third MOSFET (PMOS TP1), a fourth MOSFET (PMOS TP2), and a current block (TN31, TN32) comprising a fifth MOSFET (NMOS TN31) and a sixth MOSFET (NMOS TN32), wherein the fifth and sixth MOSFETs (TN31, TN32) having their gates connected to the low voltage power

supply (VDDL, by way of voltage divider TP3-R); an output circuit (CMOS inverter IV3) for providing an output signal (OUT); and a retainer circuit (CMOS inverter IV4). Note that, for claim 46, because the structure of the level shifter in Figure 3 of the Maejima reference is substantially similar as applicant's invention so the limitation regarding the timing operation in this claim is also met.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 35-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maejima et al. (USP 6,791,392) in view of Konishi (USP 6,373,285).

With respect to claims 35-38, the level shifter in Figure 3 of Maejima et al. meets all the limitations of these claims except that the level shifter also including seventh and eighth MOSFETs connected between the high voltage power supply and the respective third and fourth MOSFETs. However, the Konishi reference discloses Figure 1 a level shifter including PMOS transistors 14 and 15 connected between the high power supply (80) and respective PMOS transistors 16 and 17 for the purpose of controlling current flowing through the level shifter for reducing the power consumption (Col. 5, lines 33-39; Col. 9, lines 6-47). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the level shifter circuit in Figure 3 of the Maejima reference by providing a PMOS transistor (i.e., seventh MOSFET) connected between the high voltage power supply and the third MOSFET

(PMOS TP1, Figure 3 of Maejima) and another PMOS transistor (i.e., eighth MOSFET) connected the high voltage power supply and the fourth MOSFET (PMOS TP2, Figure 3 of Maejima) as taught by the Konishi reference for the purpose of reducing the power consumption of the circuitry. Thus, this modification/combination meets all the limitations of claims 35-38. Note that the gates of the seventh and eighth MOSFETs (PMOS TP1 and PMOS TP2) connected to the reference potential is also met (i.e. when control 39 connected to the gates of transistors 14 and 15 in Figure 1 of Konishi is low (ground potential) during the operation of the circuit, so the gates of PMOS 14 and 15 connected to the reference potential (ground potential)).

Response to Arguments

10. Applicant's arguments filed on 11/30/05 have been fully considered but they are not persuasive.

Applicant argues that the Maejima et al. reference fails to disclose that the gate electrode of the first transistor is configured to be supplied with a first potential of the low voltage power supply. However, this argument is not persuasive because, from Figure 3 of Maejima et al., the gates of transistors TN31 TN32 are configured to be supplied with the first potential of the low power supply VDDL (by way of voltage divider TP3-R). Note that the claim does not specifically recite that the gate of the first transistor directly receives the first potential of the low voltage power supply (or directly connected to the low voltage power supply), so for broadest reasonable interpretation, Figure 3 of Maejima et al. meets the above limitation.

Applicant also argues that Maejima et al. fails to disclose that the gates of the fifth MOSFET and sixth MOSFET are connected to the low voltage power supply. However, this argument is not persuasive because, from Figure 3 of Maejima et al., the gates of transistors

TN31 TN32 are connected to the low power supply VDDL (by way of voltage divider TP3-R). Note that the claim does not specifically recite that the gate of the fifth and sixth MOSFETs directly connected to the low voltage power supply, so for broadest reasonable interpretation, Figure 3 of Maejima et al. meets the above limitation.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

February 16, 2006

LONG NGUYEN
PRIMARY EXAMINER